UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/036,429	01/07/2002	Mitsuru Sasaki	108287-00007	4970

7590 10/05/2006

ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
1050 CONNECTICUT AVENUE, N.W., SUITE 400
WASHINGTON, DC 20036-5339

EXAMINER	
GARBOWSKI, LEIGH M	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/036,429	SASAKI, MITSURU	
	Examiner	Art Unit	
	Leigh Marie Garbowski	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-14* is/are rejected.

7)☒ Claim(s) *6,7,13 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/726,607.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/07/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Drawings

The drawings are objected to because figure 23A is an exact duplicate of figure 6A. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Figures 6A, 23A, 23B, and 24 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The abstract of the disclosure is objected to because the content describes a path transistor circuit, and not the subject matter of the present claims. Correction is required. See MPEP § 608.01(b).

The disclosure is objected to because of the following informalities: the term "path transistor(s)" must be changed to --pass transistor(s)-- throughout the entire specification.

Appropriate correction is required.

Claim Objections

Claims 6, 7, 13, 14 are objected to because of the following informalities: the term "path transistors" must be changed to --pass transistors--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 6-14 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. As per claims 6-12, taking claim 6 as exemplary, subject matter critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976). The logic specification indication unit is interpreted to be element 1 [figure 1], the cell library is interpreted to be element 700 [figure 3], and the optimization unit is interpreted to be element 3 [figure 1]. The specification discloses that the logic composition processing section conducts logic composition based on at least elements 10-12, 100, 150, 300, 350 of figure 1 [page 23, line 24-page 24, line 10]. The specification discloses that optimizing buffering includes elements 10-12 of figure 1 [page 39, lines 21-22; page 40, lines 7-12]. It is not clear that the logic composition processing section is the sole unit disclosed for optimizing buffering; the specification notes that the logic circuit is designed according to the flow chart shown in figure 8 [page 40, lines 10-12]. The specification states that the drive segment indication section [element 2] and the delay waveform and power analysis section [element 4] are structural elements necessary to practice the invention with respect to logic

composition, and that the drive segment indication section [element 2], the delay waveform and power analysis section [element 4], the automatic layout and wiring processing section [element 5], the layout data conversion section [element 6] and the delay waveform and power analysis section [element 7] of figure 1 are structural elements necessary to practice the invention with respect to optimizing buffers according to the flowchart of figure 8 [page 32, line 18-page 36, line 11]. Therefore, the claims are rejected based on the grounds that the disclosed critical elements identified above are missing from the claims; the specification makes it clear that these elements are critical for the invention to function as intended. As per claims 13-14, the same argument follows regarding the steps as claimed. The disclosed critical steps, which are considered equivalent to the sections as identified above, are missing from the claims; the specification makes it clear that these steps are critical for the invention to function as intended.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 7-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 7 and 8, the antecedent basis for "said grouped drive segments" [claim 7, line 6] and "said drive segments" [claim 8, line 3] is not clear. The language is not clear regarding what "drive segments" are.

As per claim 9, what is meant by "the select logic" [line 3] is not clear; there is no antecedent basis for this feature in claim 6, thus, what is meant by "applying" is not clear.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 14 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The specification discloses an embodiment directed to non-statutory subject matter: the computer-readable recording medium may also be a transmission medium [page 51, lines 18-21]. Thus, claim 14 is held non-statutory for failing to be directed to a statutory class of invention, given that the computer-readable recording medium includes non-statutory embodiments.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-8, 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita et al. [U.S. Patent #5,712,792] in view of Allen et al. [U.S. Patent #6,232,799].

As per claims 6, 13, 14, taking claim 6 as exemplary, Yamashita et al. teach a logic circuit optimization device for optimizing design of a logic circuit, said device comprising: a logic specification indication unit which indicates logic specifications including a plurality of control signals for controlling the plurality of pass transistors [column 7, lines 36-38]; a cell library unit which registers a plurality of cell data used to design said logic circuit [element 11; column 7, line 43]; and an optimization unit which conducts a logic composition based on the logic specifications and the cell data, and for optimizing buffering in said logic circuit [element 100; column 7, lines 36-55; column 12, lines 65-66]. However, Yamashita et al. does not specifically teach a logic circuit consisting of a plurality of pass transistors connected in parallel and having input terminals, respectively, into which input terminals a same input signal is inputted, so that a plurality of control signals controlling continuities of the plurality of pass transistors, respectively, have an exclusive relationship there between. Allen et al. teach a method and apparatus for selectively controlling pass transistor logic circuits, comprising a

plurality of pass transistors connected in parallel and having input terminals, respectively, into which input terminals a same input signal is inputted, so that a plurality of control signals controlling continuities of the plurality of pass transistors, respectively, have an exclusive relationship there between [figure 2]. Elements 202, 204, 210, 212 have input terminals into which a same input signal element A is inputted, so that a plurality of control signals elements B, B_L control continuities of the pass transistors to have an exclusive relationship there between by B_L being the inverse of B. Considering that Yamashita et al. teach a device for optimizing design of a logic circuit of a plurality of pass transistors, a person of ordinary skill in the art at the time of the invention would have found it obvious to combine these teaching to obviate the claimed invention because the negative effects of selectively controlling weak feedback in pass transistor logic circuits is substantially overcome [column 3, lines 20-26]. As per claim 7, Yamashita et al. further teach a grouping unit which groups said pass transistors into a plurality of groups [column 8, lines 24-35]. As per claim 8, Yamashita et al. further teach wherein said optimization unit optimizes buffering [column 12, line 65-66]. As per claim 10, wherein a plurality of the logic circuits are provided to constitute a macro circuit [column 12, lines 7-23]. As per claim 11, wherein a first cell data applying the maximum value of the load capacity of said logic circuit and a second cell data applying the minimum value of the load capacity are registered, as cell data for analyzing the electric characteristics of the logic circuit, in said cell library unit [column 6, lines 6-8]. As per claim 12, wherein the first and second cell data are created according to the actual operation of said logic circuit [column 17, lines 58-62].

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita et al. in view of Allen et al. as applied to claim 6 above, and further in view of Maher, III et al. [U.S. patent $5,020,013].

Maher, III et al. teach pass transistor circuits used in shifting data bits [column 8, lines 63+]. A person of ordinary skill in the art at the time of the invention would have found it obvious to have used the logic circuit as a bit shift circuit as taught by Maher, III et al. because the important technical advantage of allowing unidirectional data input with bidirectional, left and right, shifting operations is provided [column 11, lines 17-30].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leigh Marie Garbowski whose telephone number is 571-272-1893. The examiner can normally be reached on days.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LEIGH M. GARBOWSKI
PRIMARY EXAMINER